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# Technical publication

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211

## The frame-transfer sensor

With the tremendous advances in semiconductor technology over the past few years, it was only a matter of time before the solid-state image sensor (SSIS) proved itself the equal of the venerable tv camera tune. Hardly surprising when you consider its intrinsic advantages.

It causes absolutely no picture geometry distortion for a start, and it has no burn-in or lag. It's also completely unaffected by magnetic fields, and highly resistant to knocks and vibration. Add to these qualities its highly stable characteristics, its low power consumption and operating voltage, its long life and its extremely light, compact construction, and you begin to see why many tv-camera manufactures look on the SSIS as a real and attractive alternative to the camera tube.

Currently, it's use is limited to consumer, industrial and low-end broadcast applications: home video cameras, CCTV installations, industrial inspection equipment and ENG tv cameras. Rough treatment, adverse operating conditions and poor lighting are the norm in these applications, and it's here that the outstanding qualities of the SSIS really show up.

SSIS devices that offer exciting possibilities for the future are the new NXA1011 to 1041 series of frame-transfer sensors (Fig.1).

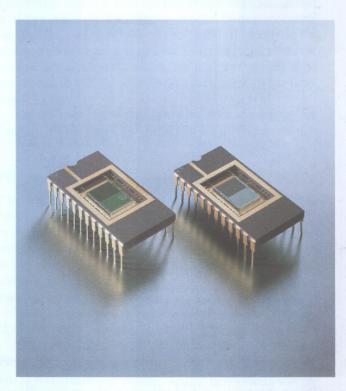
As their name suggests, these sensors operate on the frame-transfer (FT) principle, according to which each field of the complete picture frame is separately integrated within a photosensitive imaging region, transferred by CCD shift registers into a storage region during vertical blanking, and then clocked out serially to form the video signal during the subsequent field integration period.

The NXA1011 is a black/white version adapted to the CCIR standard. The NXA1021 is essentially the same device with cyan, green and yellow stripe filters to allow its use in single sensor colour tv cameras.

NXA1031 is a black/white version adapted to the EIA standard and NXA1041 the corresponding colour version.

Outstanding features of these sensors are:

- good blue sensitivity since the polysilicon gate electrodes used for clocking the CCD registers cover only about 70% of the photosensitive area
- high tolerance to overexposure which allows the devices to be used in systems where highlights are likely to be encountered, for example, surveillance installations, pipe inspection systems and ENG colour cameras (with prismatic colour-separation and three B/W sensors).



NXA1021/1041 and NXA1011/1031 frame transfer sensors. The NXA1011/1031 are black/white versions and the NXA1021/1041 incorporate stripe filters for use in single sensor colour tv cameras

### ADVANCED MOS TECHNIQUES GIVE EXTRA HIGH PIXEL DENSITY

The NXA1011 takes advantage of the latest MOS techniques that have recently provided such spectacular advances in microprocessors, memories and other complex VLSI systems. In a super-8 picture format (½-inch camera tube) with an image diagonal of no more than 7,5 mm, the device can boast a total of 294 lines, each containing 604 pixels. With the CCIR standard of 576 lines (two interlaced fields each of 288 lines), this means effectively a total of 347904 pixels (each  $10\,\mu\mathrm{m}\times15,6\,\mu\mathrm{m})$  available exclusively for imaging.

What's more, thanks to the well established production techniques now available to manufacturers of MOS devices, we can form these pixels with a uniformity hitherto undreamed of.

Figure 2 shows the FT structure of the NXA1011. It's made up of a photosensitive imaging region next to a storage region and connected to it by 604 parallel CCD shift registers. These registers are separated by stop diffusions and their width defines the pixel width.

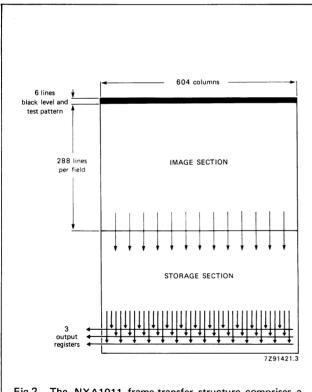


Fig.2 The NXA1011 frame-transfer structure comprises a photosensitive imaging region located next to a storage region and connected to it by parallel shift registers

A two-dimensional charge pattern representative of the image to be televised is integrated in the imaging region over the duration of a field and transferred to the storage region during the vertical blanking period.

Figure 3 shows the FT structure in more detail. The imaging and storage regions are practically identical, both being based on four-phase CCD shift registers (phases  $\phi_1$ ,  $\phi_2$ ,  $\phi_3$ , and  $\phi_4$ , subscript A in the imaging region and B in the storage region).

Charges generated by incident light in the imaging region collect beneath the gate electrodes with high potential. A low-potential electrode repels them, thus forming a boundary between charge packets to produce the individual pixels.

Figure 3 also shows the horizontal read-out structure. This comprises three 3-phase horizontal CCD shift registers controlled by gate electrodes  $\phi_{1C}$ ,  $\phi_{2C}$  and  $\phi_{3C}$ . The pixels in each line are read out in groups of three as indicated in Fig.3, selection being controlled by three transfer gates  $TG_1$ ,  $TG_2$ ,  $TG_3$ .

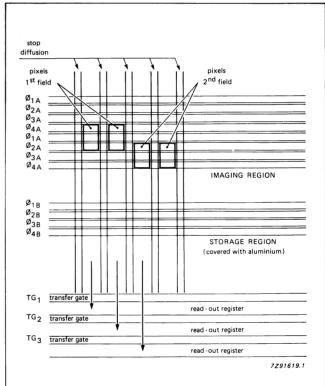
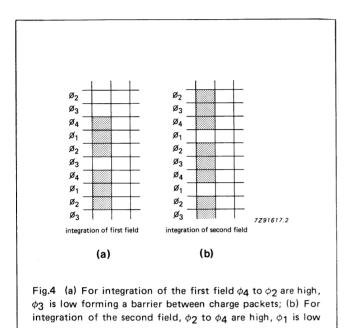


Fig.3 The imaging and storage regions are almost identical. Both incorporate four-phase CCD shift registers for vertical field transfer. Charge distribution into the three-phase horizontal readout registers is controlled by three transfer gates  $TG_1, TG_2 \ \mbox{and} \ TG_3$ 

This provides two advantages. First, it allows a much higher horizontal pixel density than would a single read-out register, in which the finite width of the gate electrodes limits the minimum horizontal spacing between charge packets. With three shift registers, this spacing is effectively reduced threefold. Second, it allows selective separation of charge packets within each line and thus, with stripe filters over the imaging region, it allows the device to be used as a colour image sensor (NXA1021/1041).

The first field is generated when the phases  $\phi_4$ ,  $\phi_1$  and  $\phi_2$  are HIGH and  $\phi_3$  is LOW, Fig.4(a).  $\phi_3$  effectively forms a potential barrier separating the pixels in the first field. The charges generated by incident light then integrate beneath  $\phi_4$  to  $\phi_2$ , centred on  $\phi_1$ .

So each pixel extends vertically over roughly three gate electrodes.

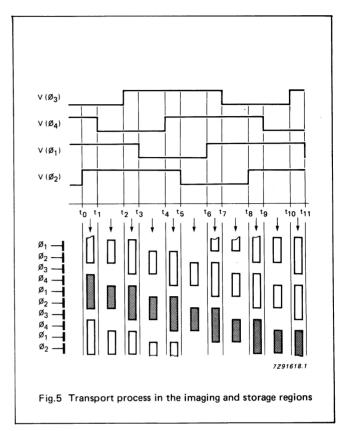


The potential distribution of the second field, and hence its position relative to the first field is shown in Fig.4(b). The second field is always displaced by two gate electrodes relative to the first field, with its charge patterns centred on  $\phi_3$  and with  $\phi_1$  forming the barrier between pixels, thus providing a perfectly interlaced frame structure.

#### FIELD TRANSFER

Figure 5 shows the transport process in the imaging and storage regions. At time  $t_0$ , the start of the first-field readout from the imaging region,  $\phi_3$  is low and the charge is concentrated beneath  $\phi_4$  to  $\phi_2$  (as described above). At  $t_1$ ,  $\phi_4$  goes low and the charge in each pixel concentrates beneath  $\phi_1$  and  $\phi_2$ . At  $t_2$ ,  $\phi_3$  goes high and the charge packets advance one gate electrode, spreading out beneath  $\phi_1$ ,  $\phi_2$  and the following electrode  $\phi_3$ . In the next step, at  $t_3$ ,  $\phi_1$  goes low compressing the charge packets beneath  $\phi_2$  and  $\phi_3$ , and at  $t_4$ ,  $\phi_4$  goes high allowing the charge packets to again advance one gate electrode.

This process continues in both the imaging and storage regions until all the charge packets have transferred to the storage region.



#### HORIZONTAL READ-OUT

The storage region is read out line-by-line while integration is taking place in the imaging region. During successive horizontal-blanking periods, the vertical shift-registers in the storage region advance the stored image one line, so that at the end of the blanking period, the next line is ready to be transferred to the horizontal read-out registers via the three transfer gates.

The read-out registers are provided with an output stage (source follower) with a sensitivity of  $3.5 \mu V$  per electron.

#### PULSE SEQUENCES FOR THE NXA1011/1021

Figure 6 shows the drive-pulse sequence and line numbering for field-transfer in the NXA1011/1021 (for the PAL/CCIR tv standard). To show both fields in the same figure, the second field is shown below the first with the appropriate tv line numbering above it. As the figure shows, the field-transfer process occupies about 30% of the tv-standard vertical blanking period.

The CCD lines used for image recording are distinguished in the figure by hatching and by the letter 'V' above them.

The read-out time for the first field extends from tv lines 23 to 310, and for the second field from tv lines 336 to 623. Lines 624 to 3, and lines 311 to 315 are all shifted out but not transmitted. Lines 314 and 2 serve as black-level reference lines, and lines 312 and 624 are all reserved for testing the sensor during production.

Figure 7 shows the field-transfer pulses in greater detail, as well as the transfer-gate pulses and the horizontal readout pulses  $\phi_{1C}$ ,  $\phi_{2C}$  and  $\phi_{3C}$ . Transfer gates TG<sub>2</sub> and TG<sub>3</sub> are connected electrically, so only the former's pulse sequence is shown.

Since the first field is shifted relative to the second by half a line, to bring it into the correct position for transfer into the storage region, half a clock period must be added at the start and end of its  $\phi_A$  pulses (Fig.7(a)).

Transfer gate  $TG_1$  is closed during the waiting period, i.e. the period between transfer of a field into the storage region and the start of readout of that field (see Figs 6 and 8).

The last gate electrode in the storage region is  $\phi_{3B}$ , and this is followed by  $TG_1$  which controls transfer of the signal charge from the storage region into the upper horizontal read-out register. During the horizontal blanking period, pulses  $\phi_{3B}$ ,  $TG_1$ ,  $TG_2$ , in combination with  $\phi_{1C}$  to  $\phi_{3C}$  (Fig.9) sort the signal charge into the three horizontal read-out registers.

At the end of each field read-out, all residual charge in the storage region must be removed before the next field is entered. This is done by keeping  $TG_1$  open after the field has been clocked out and continuing to clock the horizontal registers (phases  $\phi_C$ ) until the next field is ready to be read out.

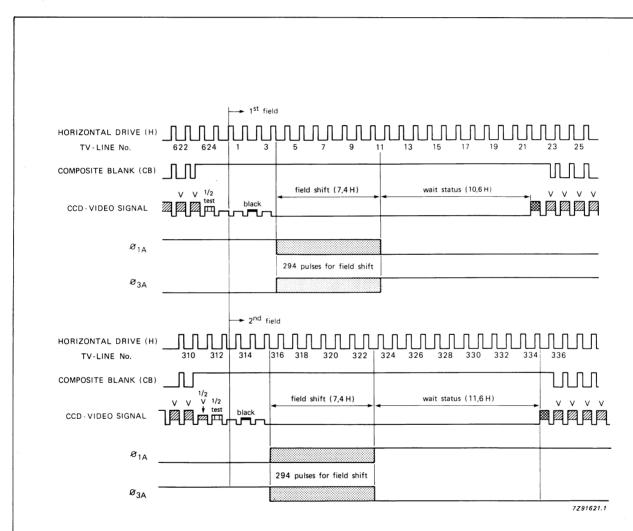
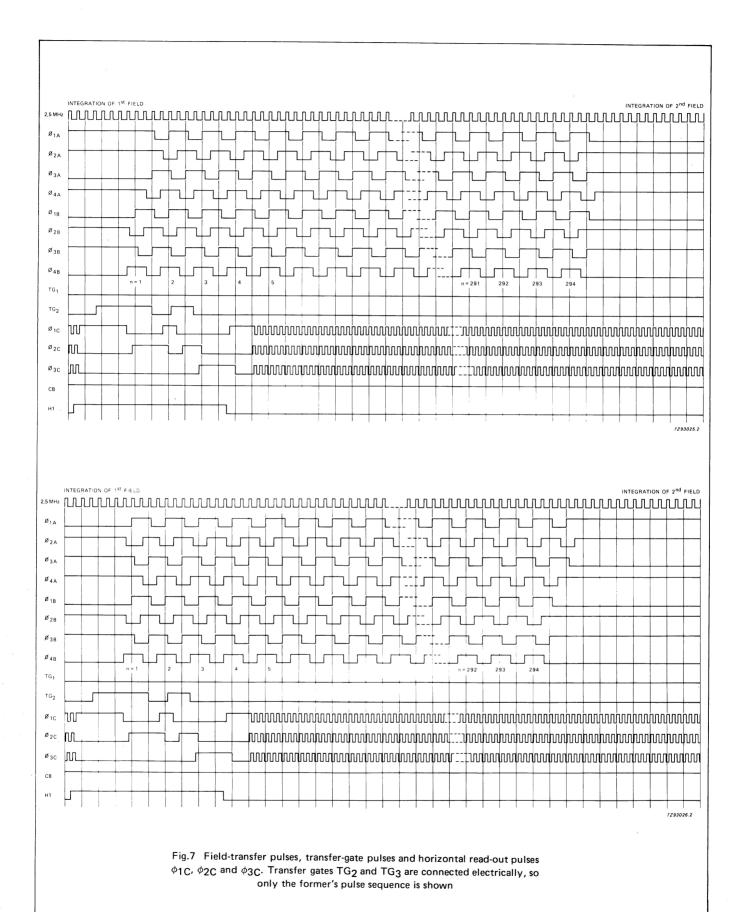


Fig.6 Drive-pulse sequence and line numbering for field transfer (PAL/CCIR tv standard). Of the  $\phi_A$  pulses, only  $\phi_{1A}$  and  $\phi_{3A}$  are shown since these pulses change sign between the first and second fields. The actual details of the  $\phi_A$  pulses can be found in Fig.5



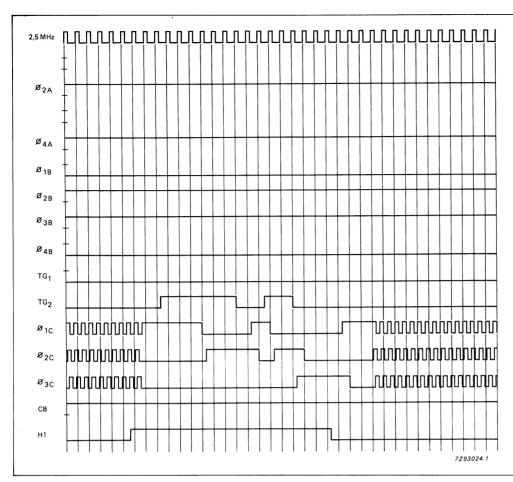


Fig.8 Transfer gate TG<sub>1</sub> is closed during the waiting period, i.e. the period between field transfer into the storage region and the start of readout of that field

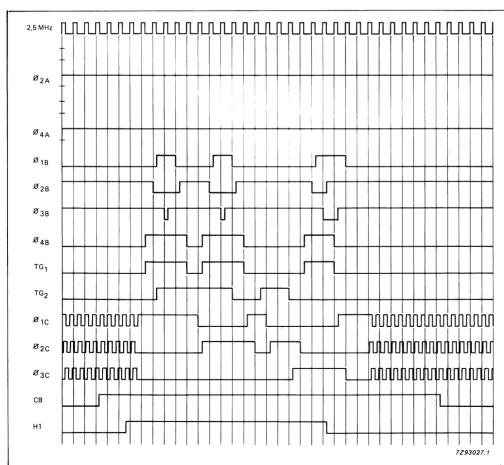


Fig.9 During the horizontal blanking period, pulses  $\phi_{3B}$ , TG<sub>1</sub>, TG<sub>2</sub> and  $\phi_{1C}$  to  $\phi_{3C}$  sort the signal charge into the three horizontal read-out registers

#### DRIVE CIRCUIT FOR THE NXA1011/1041

Figure 10 shows a circuit for providing the pulse sequences needed to drive the NXA1011 to 1041 series.

An SAA1043 sync-pulse generator, provides pulses for the three tv standards, namely PAL, SECAM and NTSC. These include vertical and horizontal blanking and blacklevel clamping. It also provides other signals essential for tv camera operation, and can be triggered externally for operation with, for example, a VCR or computer.

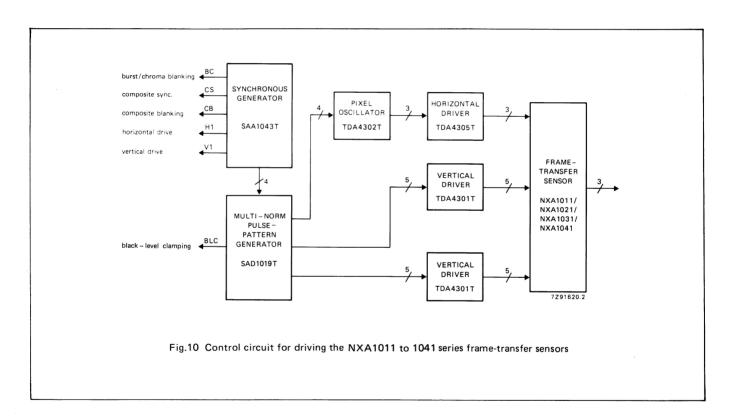
The sync-pulse generator drives an SAD1019\* multinorm pulse-pattern generator, developed specifically for the NXA1011 to 1041. It provides all the clock signals except the pulses for the horizontal read-out registers, and its use avoids the need to develop complex circuitry for driving the NXA1011 to 1041.

Fast clock pulses for the three horizontal read-out registers are generated by a TDA4302, 'pixel oscillator'

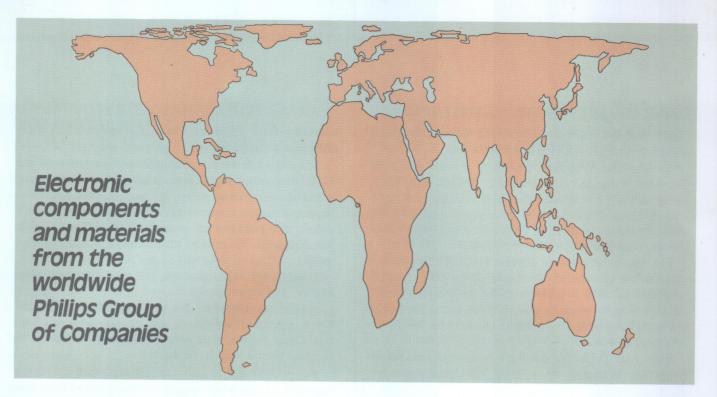
delivering three 3,9 MHz pulse trains with a 120° phase difference between them.

The output levels from the pulse-pattern generator and from the pixel oscillator are too low to drive the shift registers directly. Extra driver ICs are therefore needed to boost the signals: for the pixel oscillator — one TDA4305, and for the pulse-pattern generator — two TDA4301 ICs. The TDA4301 ICs are also used to boost the transfer-gate pulses.

During horizontal blanking, the pixel oscillator is inhibited, and slower pulses derived from the pulse-pattern generator are applied to the pixel-oscillator output, and hence, via the TDA4305, to the transfer gates and horizontal gate electrodes to sort the charge packets into the three horizontal read-out registers.



<sup>\*</sup> Previously SAD1008.



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